CLAIMS:

1. A system comprising:

a memory having linearly addressable storage units to store video data; and

a programmable video direct memory access (VDMA) controller to access the storage units of the memory in response to a command specifying a multidimensional block of video data.

2. The system of claim 1, wherein the command specifies a number of rows and a number of columns for the block of video data.

3. The system of claim 1, wherein the command specifies a jump parameter indicating a number of storage units between each row of the video block.

4. The system of claim 1, wherein in response to the command, the VDMA controller copies the video data from the memory to a destination memory.

5. The system of claim 4, wherein the command specifies a starting address of the video block within the memory, and a starting address within the destination memory.

6. The system of claim 1, wherein the VDMA controller fetches from the memory an entire block of video data having multiple non-contiguous rows in response to the command.

7. The system of claim 1, further comprising:

a processor to issue commands to the VDMA controller via a first bus; and

a digital signal processor to issue commands to the VDMA controller via a second bus.

8. The system of claim 1, further comprising a motion estimation unit having an internal memory and a differential calculator to calculate a distortion metric between blocks of video data, wherein the VDMA controller copies blocks of video data from the memory to the internal cache of the motion estimation unit in response to the command.

9. A method comprising:

receiving a direct memory access (DMA) command from a processor to transfer a multidimensional block of video data;

generating a set of source addresses and a set of destination addresses in response to the command; and

copying video data from a source memory to a destination memory according to the source addresses and destination addresses.

10. The method of claim 9, wherein the source memory and the destination memory each have linearly addressable storage units.

11. The method of claim 9, wherein the command specifies a number of rows and a number of columns for the block of video data, and wherein generating a set of addresses comprises calculating the source addresses and destination addresses as a function of the number of rows and the number of columns.

12. The method of claim 9, wherein the command specifies a jump parameter indicating a number of addresses between each row of the video block, and wherein generating a set of addresses comprises calculating the source addresses and destination addresses as a function of the jump parameter.

13. The method of claim 9, wherein the command specifies a starting source address of the video block within the source memory, and a starting destination address within the destination memory.

14. The method of claim 9, wherein copying video data comprises fetching an entire block of video data having multiple rows in response to the command.

15. The method of claim 9, wherein receiving the command comprises receiving the command via a first bus, the method further comprising receiving a second command from a digital signal processor via a second bus.

16. The method of claim 9, wherein copying video data comprises copying the video data to an internal cache of a motion estimation unit in response to the command.

17. A device comprising:

a first memory to store a candidate video block to be encoded;

a second memory to store a set of video data blocks from which to encode the candidate video block; and

a differential calculator to calculate differential metrics between the candidate video block and the set of video blocks.

18. The device of claim 17, wherein the set of video data blocks stored by the second memory comprises a complete video data frame.

19. The device of claim 17, wherein the differential calculator includes address generation logic to read the candidate video block from the first cache and one or more video blocks of the set of video blocks from the second cache.

20. The device of claim 19, wherein the differential calculator reads the candidate video block from the first cache and one or more video blocks of the set of video blocks from the second cache in parallel.

21. The device of claim 17, further comprising a programmable video direct memory access (VDMA) controller to copy the candidate video block and the set of video blocks from a video memory to the first cache and the second cache, respectively.

22. The device of claim 21, wherein the VDMA controller copies the set of blocks to the second cache in response to a single direct memory access (DMA) command specifying a multidimensional search space of video data within the video memory.

23. The device of claim 22, wherein the command specifies a number of rows and a number of columns for the search space of video data.

24. The device of claim 21 wherein the video memory includes a plurality of linearly addressable storage units to store video data.

25. The device of claim 21, wherein the command specifies a jump parameter indicating a number of storage units between each row of the video block.

26. The device of claim 21, wherein the command specifies a starting source address of the video block within the video memory, and a starting destination address within the second cache.

27. The device of claim 21, wherein the VDMA controller fetches the search space having multiple non-contiguous rows in response to the command.

28. The device of claim 21, further comprising:

a processor to issue commands to the VDMA controller via a first bus; and

a digital signal processor (DSP) to issue commands to the VDMA controller via a second bus.

29. The device of claim 17, wherein the differential calculator calculates the differential metrics in response to search commands, and wherein each search command specifies a multidimensional region of video data stored within the second memory.

30. The device of claim 29, further comprising a command buffer to store the search commands and deliver the search commands to the differential calculator.

31. A device comprising:

means for receiving a direct memory access (DMA) command from a processor to transfer a multidimensional block of video data;

means for generating a set of source addresses and a set of destination addresses in response to the command; and

means for copying video data from a source memory to a destination memory according to the source addresses and destination addresses.

32. The device of claim 31, wherein the source memory and the destination memory each have linearly addressable storage units.

33. The device of claim 31, wherein the command specifies a number of rows and a number of columns for the block of video data, and wherein the generating means comprises means for calculating the source addresses and destination addresses as a function of the number of rows and the number of columns.

34. The device of claim 31, wherein the command specifies a jump parameter indicating a number of addresses between each row of the video block, and wherein the generating means comprises means for calculating the source addresses and destination addresses as a function of the jump parameter.

35. The device of claim 31, wherein the command specifies a starting source address of the video block within the source memory, and a starting destination address within the destination memory.

36. The device of claim 31, wherein the copying means comprises means for fetching an entire block of video data having multiple rows in response to the command.

37. The device of claim 31, wherein the receiving means receives the command via a first bus and a second command from a digital signal processor via a second bus.

38. The device of claim 31, wherein the copying means comprises means for copying the video data to an internal cache of a motion estimation unit in response to the command.